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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,178	08/30/2006	Pierre Blanchard	4590-556	7764
33308	7590	09/04/2007		EXAMINER
LOWE HAUPTMAN & BERNER, LLP				GUMEDZOE, PENIEL M
1700 DIAGONAL ROAD, SUITE 300				
ALEXANDRIA, VA 22314			ART UNIT	PAPER NUMBER
			2891	
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			09/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/591,178	BLANCHARD, PIERRE
	Examiner Peniel M. Gumedzoe	Art Unit 2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 30 August 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-5 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 30 August 2006 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>08/30/2006</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on August 30, 2006 was received by the examiner before the issuance/mailing date of the first office action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

Claim Objections

3. Claim 2 is objected to because of the following informalities: Claim 2 recites "... the silicon is subsequently oxidized over its entire thickness wherever it is not covered with nitride, until a silicon pattern is obtained which comprises only the zones that were not covered with nitride". It is not understood how the zones that were not covered with nitride will still have silicon after a full thickness oxidation. The claim seems to contradict page 11, lines 9-10. Examiner thus assumed that the silicon is converted to oxide wherever it is not covered by nitride. Examiner also suggests that applicant correct the ambiguity.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamimura et al. ('565) and further in view of Kub ('604).

Kamimura et al. ('565) disclose a method for fabricating a diode comprising: producing two electrodes separated by a gap above a substrate, forming an insulator layer over the electrodes and exposing the space between the two electrodes, depositing a layer of doped polycrystalline silicon in the space entering in contact with the substrate and selectively patterning the polycrystalline silicon, depositing an insulating layer above the polycrystalline silicon and locally etching an opening in the insulating layer outside the space lying between the electrodes, depositing and etching a metal to form a contact with the polycrystalline through the opening (see Fig. 1 and column 2 lines 26-63 of '565). But Kamimura et al. ('565) do not appear to explicitly disclose thermally oxidizing the electrodes to form the electrodes insulating layer.

However Kub ('604) discloses oxidizing electrodes to form insulating layers (see Fig.2 and column 5 lines 55-68 of '604).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have formed polysilicon electrodes and oxidized them to form the insulating film 6 of the device of '565. One would have been motivated to do so

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because it is a simple and commonly known way of forming insulating layer on polycrystalline silicon (this is also admitted by applicant).

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamimura et al. ('565) and Kub ('604) and further in view of Zoroglu ('535).

Kamimura et al. ('565) and Kub ('604) disclose all the limitations of claim 1 as stated above but do not appear to explicitly disclose using nitride as insulating layer above the doped polysilicon, leaving uncovered and covered portions of the doped polysilicon layer and oxidizing the doped polysilicon layer until a silicon pattern is obtained which comprises only the covered zones.

However Zoroglu ('535) discloses oxidizing polysilicon layer having covered (with a passivation layer) and uncovered portions to form electrodes (see Figs. 6-9 and column 4 line 23 through column 5 lines 1-30 of '535).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have used silicon nitride as passivation layer and formed the doped polysilicon electrode according to the method of '535. One would have been motivated to do so because silicon nitride is a commonly used passivation layer for electrodes in Microfabrication and the oxidation step would have avoided the etching step for removing uncovered portions of the doped polysilicon electrode.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamimura et al. ('565), Kub ('604), Zoroglu ('535) and further in view of Wolf (Silicon Processing for the VLSI Era, page 331).

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Kamimura et al. ('565), Kub ('604) and Zoroglu ('535) disclose all the limitations of claim 2 as stated above but do not appear to explicitly disclose chemically attacking the unprotected portions of the doped polysilicon in order to remove it as much as possible before to oxidation step.

However Wolf discloses partially etching unprotected portions of a silicon layer before oxidizing (see page 331 of Wolf).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have partially etched the unprotected portions of the doped polysilicon before oxidizing the polysilicon layer. One would have been motivated to do so because doing so would have allowed the oxidized portions to have planar surface with the protected portions (see the first paragraph on page 331 of Wolf).

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens ('990) and further in view of Kamimura et al. ('565).

Stevens disclosed an integrated circuit comprising a CCD register with a readout diode at the end of the register, between the last electrode of the register and a reset electrode wherein the readout diode includes a doped region delimited on one side by the electrodes and on the other side by region of thick silicon oxide (see Figs. 1-4 and 6, column 2 lines 44 through column line 68, column 4 line 63 through column 5 line 2 of '990). But Stevens ('990) does not appear to explicitly disclose the doped region being entirely covered with a layer of polycrystalline silicon delimited according to a pattern which extends partly above the thick oxide (it rather teaches aluminum in column 4 lines

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63-64), an insulating layer covering the silicon pattern and having an opening not located above the doped region, and a conductive layer above the insulating layer and in contact with the silicon layer through the opening.

However, Kamimura et al. ('565) disclose an insulating layer covering a doped polycrystalline silicon pattern and having an opening not located directly above the doped contact region, and a conductive layer above the insulating layer and in contact with the silicon layer through the opening (see Fig. 1 and column 2 lines 26-63 of '565).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have used doped polycrystalline (instead of aluminum), covered the polycrystalline silicon pattern and made an opening not located directly above the doped contact region, and to have formed a conductive layer above the insulating layer and in contact with the silicon layer through the opening. One would have been motivated to do so in order to provide interconnect contact for the diode and also because the doped polycrystalline is a functional equivalent of Aluminum.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens ('990), Kamimura et al. ('565) and further in view of Spangler et al. ('064).

Stevens ('990) and Kamimura et al. ('565) disclose all the limitations of claim 4 as stated above but do not appear to explicitly disclose the polycrystalline layer covered with silicon nitride, itself covered by an insulating layer and both nitride and insulating film having an opening located at the same position.

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However, Spangler et al. ('064) disclose using nitride layer to cover doped polysilicon to prevent diffusion of impurities (see layer 160 on Fig. 5 and column 12 lines 50-64 of '064).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have covered the doped polycrystalline silicon pattern (in the device as per claim 4 rejection) with a silicon nitride layer, itself covered by the insulating film 8 and made a hole through both layers to allow contact with conductive layer 9 (see Fig. 1 of '565 and column 2 lines 53-62). One would have been motivated to do so to prevent impurities diffusion.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Nakashiba et al. discloses a method of making CCD image sensor where polysilicon electrodes are thermally oxidized

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peniel M. Gumedzoe whose telephone number is 571-270-3041. The examiner can normally be reached on M-F from 9:30 AM to 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister, can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 26, 2007

Peniel Gumedzoe

Examiner / Art Unit 2891



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